EE 330

Assignment 1 Solutions Fall 2022

1)

First, we need to find the area of one of these transistors:

Transistor Area (TA) = $5nm * 5nm = 25nm^2$

Transistor Area + Overhead = $TA * 10 = 250nm^2$

Now we need to get an idea of the area of the wafer to find roughly how many dies can be on it:

Wafer Radius (R) = $\frac{diameter}{2} = \frac{300mm}{2} = 150mm$

Wafer Area (A) = $\pi R^2 = 70650mm^2 = 7.065 \times 10^{16} nm^2$

Die Area (DA) = $2750 * (TA + overhead) = 687500nm^2$

To make things easier, I will convert mm^2 and nm^2 to m^2. ($1nm^2 = 10^{-18}m$ and $1mm^2 = 10^{-6}m$)

Number of Die = $\frac{Wafer\ Area}{Die\ Area} = 1.027 * 10^{11} \frac{dies}{wafer}$

2)

$$\frac{Cost}{die} = \frac{7250 \frac{\$}{wafer}}{1.027 * 10^{11} \frac{dies}{wafer}} = 7.05 * 10^{-8} \frac{\$}{die}$$

3)

A silicon atom has an atomic diameter of approximately $210pm$, which is equivalent to $0.21nm$. This means that a $5nm$ transistor is approximately 23.8 times larger than a single silicon atom.

A silicon dioxide molecule has a diameter which is roughly equal to $1nm$. This means that a $5nm$ transistor is approximately 5 times larger than a SiO2 molecule.

Depending on a number of factors, the width of a human hair is approximately $100\mu m$. This means that a human hair is approximately 20,000 times larger than a $5nm$ transistor.

4)

There are a number of reasons why it is more energy efficient to use multiple cores on a die operating at a lower frequency than to use a single core operating at a high frequency. The main reasons are that the power dissipation of a circuit increases with operating frequency and that, if multiple cores are used, unnecessary cores can be deactivated. Deactivating unused cores saves a significant amount of power.

5)

If the numbers vary it is ok. The goal is to get estimates to see the size of semiconductor manufacturing companies.

Samsung: 206 Billion Dollars (statistica.com)

Intel: 77.9 Billion Dollars (intc.com)

Boeing: 76.6 Billion Dollars (statistica.com)

Nestle: 92.2 Billion Dollars (investopedia.com)

6)

(a) $I = \frac{P}{V} = \frac{95W}{1.2V} = 79.2A$

(b) For a gold wire with 1mil diameter, resistivity $\rho = 1.16\Omega/inch$ and the current from part (a)

$R = \rho L = 0.58\Omega$

$V = I * R = 45.9V$

(c) $P = I^2 R = 3638W$

(d) $\#\ of\ wires = \frac{total\ current}{current\ per\ wires} = \frac{79.2}{0.06} \sim \frac{79.2}{0.07} = 1131 \sim 1320\ wires$

7 - 8)

Type	**Storage Density (Bit/cm²)**	**Cost of Storage ($/bit)**	
CD	107	10−11	
DVD	108	10−12	Lowest
Blue Ray	109	10−12	Lowest
Hard Disk	1010	10−12	Lowest
SRAM	107	10−6	Highest
DRAM	109	10−9	
FLASH	1010	10−10	

$$Ratio = \frac{10^{-6}}{10^{-12}} = 106$$

9)

Per https://www.eweek.com/:

Android: 85%

iOS: 13%

Windows: 0.04%

10)

1.39 billion handsets shipped in 2021 (https://www.cnbc.com/2022/01/28/global-smartphone-shipment-grew-for-first-time-since-2017-counterpoint.html)

15 billion mobile devices operating worldwide (https://www.statista.com/statistics/245501/multiple-mobile-device-ownership-worldwide/)

Android at 69.71%, iOS at 29.51%, other at 0.73% (https://gs.statcounter.com/os-market-share/mobile/worldwide)

Percent phones replaced this year = 1.39 billion / 15 billion = 9.267%

Making a lot of assumptions, it appears that roughly 9% of people replaced their cell phones in 2021. That being said, this implies every phone purchase is a replacement and that everyone owns one phone. Even making those assumptions, this means that many people are either content with their current phone, content with not owning a phone, or in a position where a replacement phone is not within reach.

11)

Revenue of mobile phone sales = $500 * 1.39 billion = $695 billion

Number of full-time engineers = $695 billion / $85000 = 8,176,470

12)

a) Hint: Don't count the wafers on the die. It's not fun. Instead, just Google the estimated area of a skylake chip and divide by the area of the wafer. Ignore edge cases.

Area of wafer = πr^2 = π(225mm)^2 = 159,043 mm^2

Estimated area of skylake wafer = 332mm^2 (https://www.anandtech.com/show/11550/the-intel-skylakex-review-core-i9-7900x-i7-7820x-and-i7-7800x-tested/6)

Estimated skylake chips/wafer = $\frac{159{,}043mm^2}{332mm^2} = 479.045$

Rounding, this gives us 479 skylake chips per 450mm wafer

b) Total functional chips per wafer = $479 * .9 \cong 431$

cost per chip = $\frac{\$7500}{431} = \$17.40$

13)

USB 2.0 - 4 Conductors: VBus, Data+, Data-, Gnd

USB 3.0 - 9 Conductors: VBus, Data+-, Gnd, GND_DRAIN, and two differential pairs of RX/TX transceivers

Backwards compatibility is achieved by retaining the Data+ and Data- pins in the USB 3.0 connector. Additionally, test signals/messages can be sent from one USB-C port controller to check if the other end of the connection's controller also follows the USB-C protocol and adapt as needed.